6. (Amended) The pattern synchronous circuit as defined in claim 1 wherein the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

Add the following new claims:

7. (New) The pattern synchronous circuit as defined in claim 3 wherein said shift means shifts bits without sorting a list of the parallel signals according to the frame position information.

8. (New) The pattern synchronous circuit as defined in claim 3 wherein said sort means sorts a list of bits in the same clock of the parallel signals according to the frame position information.

9. (New) The pattern synchronous circuit as defined in claim 2, wherein the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

10. (New) The pattern synchronous circuit as defined in claim 3, wherein the low order bit of the frame position information outputted by said frame detection means has the number of bits sufficient to indicate values of the number m of shift means constructing said second sort means.

REMARKS

Claims 4, 5 and 6 have been amended to remove multiple dependencies.

Claims 1-10 are pending.

Applicant submits that all of the claims are in condition for examination, which action is requested. Please apply any other charges or credits to Deposit Account